

REMARKS

This paper is being provided in response to the Office Action mailed March 19, 2004, for the above-referenced application. In this response, Applicant has amended claims 6 and 9 and added new claims 15-25 to clarify that which Applicant considers to be the invention. Further, Applicant submits herewith a substitute specification under 37 C.F.R. 1.125 and has amended the specification and drawings for purposes of clarification. Applicant respectfully submits that the amendments to the claims and the new claims are fully supported by the originally-filed specification and that the amendments to the specification and drawings do not add new subject matter.

The objection to the drawings have been addressed by amendments contained herein as explained above. Accordingly, Applicant respectfully requests that this objection be reconsidered and withdrawn.

The objections to the specification are address herein according to the guidelines as set forth in the Office Action. Applicant submits herewith a substitute specification under 37 C.F.R. 1.125 having a 12 point font size as required by the Examiner. Applicant respectfully submits that the substitute specification does not add any new matter. Further, Applicant has amended the substitute specification, as noted above, to duplicate amendments that were previously made to the original specification by preliminary amendment and to address the objections set forth in the Office Action. Accordingly, Applicant respectfully requests that these objections be reconsidered and withdrawn.

The rejection of claims 6-8 under 35 U.S.C. 102(e) as being anticipated by Applicant's admitted prior art Figure 1-4 (hereinafter "Applicant's APA") is hereby traversed and reconsideration is respectfully requested.

Independent claim 6, as amended herein, recites a semiconductor device. The device includes a substrate and a first dielectric film overlying the substrate, said first dielectric film having a pair of trenches formed therein apart from each other. A pair of fuse terminals are embedded in an associated one of said pair of trenches of the first dielectric film. A fuse element is formed on the second dielectric film in electrical contact with the pair of fuse terminals through the openings. Claims 7 and 8 depend on independent claim 6.

Applicant's APA discloses a fuse block 10 including a pair of fuse terminals 18A and 18B and a fuse element 12, which are formed on an underlying dielectric film 14 as a common layer with interconnect lines such as signal lines 16A, 16B and 16C.

Applicant's independent claim 6, as amended herein, recites at least the features of a semiconductor device including a pair of fuse terminals each embedded in an associated one of a pair of trenches of said first dielectric film. (See, for example, Figure 8 of the present application.) Applicant's have clarified that the pair of fuse terminals are embedded in trenches formed in said first dielectric film.

Applicant respectfully submits that Applicant's APA does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Applicant's APA does not show trenches

for embedding the fuse terminals therein. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 9-11 under 35 U.S.C. 103(a) as being unpatentable over Applicant's APA in view of U.S. Patent No. 5,731,624 to Mostiff et al. (hereinafter "Mostiff") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 9, as amended herein, recites a semiconductor device including a substrate. A first dielectric film overlies the substrate. A pair of fuse terminals are embedded in a surface portion of said first dielectric film. A fuse element is formed on the first dielectric film and connected to the pair of fuse terminals. A second dielectric film is formed to cover the first dielectric film and the fuse element. A third dielectric film is formed on the second dielectric film and an opening is formed in the third dielectric film to expose a part of the second dielectric film above the fuse element. Claims 10-11 depend on independent claim 9.

The Mostiff reference discloses an integrated pad and fuse structure for planar copper metallurgy. The Office Action cites Mostiff as disclosing multiple dielectric film layers.

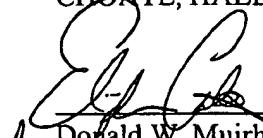
Applicant's independent claim 9, as rewritten herein, recites at least the features that second and third dielectric films are formed, respectively, on a substrate and openings are formed on the third dielectric film to expose portions of the second dielectric film overlying the fuse element. See, for example films 54, 58 and openings 59 of Figure 8 of the present specification.

Applicant respectfully submits that neither Applicant's APA nor the Mostiff reference disclose at least the above-noted features as claimed by Applicant. In particular, Applicant's APA does not disclose the features of multiple dielectric films as recited by the present claimed invention, and although the Office Action cites Mostiff as disclosing a second dielectric film, Mostiff does not make any mention of a third dielectric film nor openings formed therein to expose portions of the second dielectric film as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Further, Applicants have added new claims 15-25 and respectfully submit that these claims are patentable over the prior art of record.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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